PTO/SB/08B (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Buchty et al.
Art Unit	
Examiner Name	
Attorney Docket Number	Buchty 1-7-1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		R. ESPASA, M. VALERO, J. SMITH, Vector Architectures: Past, Present and Future, International Conference on Supercomputing (ICS'1998), pp. 425-432, July 1998	
		Pages downloaded from home.ecn.ab.ca/~jsavard/other/arcint.htm,ar02.htm,ar0201.htm,ar0202.htm,ar020201.htm,ar0302htm,ar0304.htm; downloaded on 11/24/03	
		P. KOOPMAN, Vector Architecture, Carnegie Mellon 18-548/15-548 Memory System Architecture, 11/4/98, downloaded from www.ece.cmu.edu/~ece548/handouts/16v_arch.pdf on 11/24/03	
		W. BUCHHOLZ, The IBM System/370 vector architecture, IBM Systems Journal, Vol. 25, No. 1, 1986, pp. 51-62	
		M. MITTAL, A. PELEG, U. WEISER, MMX Technology Architecture Overview, Intel Technololgy Journal, 3rd Quarter 1997, www.intel.com/technology/itj/q31997/pdf/archite.pdf	
		A. PELEG, U. WEISER, MMX Technology Extension to the Intel Architecture, IEEE Micro, 1996, pp. 42-50	
		Motorola, AltiVec Technology At-a-Glance, 2002, downloaded from http://e-www.motorola.com/files/32bit/doc/fact_sheet/ALTIVECGLANCE.pdf	
		S. FULLER, Motorola's AltiVec Technology, 1998, downloaded from http://e-www.motorola.com/files/32bit/doc/fact_sheet/ALTIVECWP.pdf	
		Motorola, AltiVec Execution Unit and Instruction Set Overview, downloaded from http://e-www.motorola.com/webapp/sps/site/overview.jsp?nodeId=03C1TR0467mKqW5Nf2hG12 11/24/03	
		V. FISCHER, M. DRUTAROVSKY, Scalable RSA Processor in Reconfigurable Hardware - a SoC Building Block, Conf. on Design of Circuits and Integrated Sys., 11/ 20-23/01, Portugal	

Examiner Signature		Date Considered	

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		Hewlett Packard, VAX MACRO and Instruction Set Reference Manual, sections 10.10-12, April 2001	
		R. BUCHTY, Cryptonite - A Programmable Crypto Processor Architecture for High-Bandwidth Applications, Thesis, Technische Universitat Munchen, January 10, 2003	

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